REMARKS

Claims 1-35 were examined and reported in the Office Action. Claims 1-35 are rejected. Claim 8 is canceled. Claims 1, 4, 9, 11, 14-15, 17, 20, 29 and 32 are amended. Claims 1-7 and 9-35 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I.   In The Drawings

The drawings are objected to because they do not show every feature of the invention specified in the claims and other informalities. Applicant has amended Figures 6 and 9 to overcome the aforementioned objections. Approval is respectfully requested.

II.   35 U.S.C. §103

A.   It is asserted in the Office Action that claims 1-7, 9-13, 17-19, 27 and 29-35 are rejected under 35 U.S.C. §103(a) as being unpatentable over by Sundaramoorthy et al. ("Slipstream Processors: Improving both Performance and Fault Tolerance", ASPLOS, pp. 257-268, Nov. 2000) ("Sundaramoorthy") in view of Hennessy and Patterson ("Computer Architecture A Quantitative Approach", Morgan Kaufmann, 1996) ("Hennessy"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation

of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "[a] apparatus comprising: a first processor and a second processor each having a scoreboard and a decoder; a plurality of memory devices coupled to the first processor and the second processor; a first buffer coupled to the first processor and the second processor, the first buffer being a register buffer; a second buffer coupled to the first processor and the second processor, the second buffer being a trace buffer; and a plurality of memory instruction buffers coupled to the first processor and the second processor; wherein the first processor and the second processor perform single threaded applications using multithreading resources, and the first processor executes a single threaded application ahead of the second processor executing said single threaded application to avoid misprediction."

Applicant's amended claim 11 contains the limitations of "[a] method comprising: executing a plurality of instructions in a first thread by a first processor; executing said plurality of instructions in the first thread by a second processor as directed by the first processor, the second processor executing said plurality of instructions ahead of the first processor to avoid misprediction; tracking at least one register that is one of loaded from a register file buffer, and written by said second processor, said tracking executed by said second processor, transmitting control flow information from the second processor to the first processor, the first processor avoiding branch prediction by receiving the control flow information; transmitting results from the second processor to the first processor, the first processor avoiding executing a portion of instructions by committing the results of the portion of instructions into a register file from a first buffer, the first buffer being a trace buffer,

and clearing a store validity bit and setting a mispredicted bit in a load entry in the first buffer if a replayed store instruction has a matching store identification (ID) portion in a second buffer, the second buffer being a load buffer."

Applicant's amended claim 20 contains the limitations of "[a] n apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising: executing a first thread from a first processor; executing said first thread from a second processor as directed by the first processor, the second processor executing instructions ahead of the first processor to avoid misprediction; tracking at least one register that is one of loaded from a first buffer, and written by said second processor, said tracking executed by said second processor, the first buffer being a register file buffer, and clearing a store validity bit and setting a mispredicted bit in a load entry in a second buffer if a replayed store instruction has a matching store identification (ID) portion, the second buffer being a trace buffer."

Applicant's amended claim 29 contains the limitations of "[a] system comprising: a first processor and a second processor each having a scoreboard and a decoder; a bus coupled to the first processor and the second processor; a main memory coupled to the bus; a plurality of local memory devices coupled to the first processor and the second processor; a first buffer coupled to the first processor and the second processor, the first buffer being a register buffer; a second buffer coupled to the first processor and the second processor, the second buffer being a trace buffer; and a plurality of memory instruction buffers coupled to the first processor and the second processor, wherein the first processor and the second processor perform single threaded applications using multithreading resources, and the first processor executes a single threaded application ahead of the second processor executing said single threaded application to avoid misprediction."

Sundaramoorthy discloses a multiprocessor system that executes pseudo-redundant programs on separate processors on the same chip. The redundant programs, however, have different amount of instructions. That is, one of the programs

has more instructions than the other. (Sundaramoorthy, page 258, first column, lines 40-55). And, both programs run in parallel on two processors. Sundaramoorthy, however, does not teach, disclose or suggest "the first processor executes a single threaded application ahead of the second processor executing said single threaded application to avoid misprediction," "executing a plurality of instructions in a first thread by a first processor; executing said plurality of instructions in the first thread by a second processor as directed by the first processor, the second processor executing said plurality of instructions ahead of the first processor to avoid misprediction," nor "executing a first thread from a first processor; executing said first thread from a second processor as directed by the first processor, the second processor executing instructions ahead of the first processor to avoid misprediction." That is, the same thread is run twice, where one thread is executed in advance of the other. Since the same thread is ran, it is obvious that both the first processor and the second processor execute the same amount of instructions.

Further, it is asserted in the Office Action that Sundaramoorthy discloses a delay buffer that operates as a trace buffer. Sundaramoorthy, however, does not disclose, teach or suggest "<u>a first buffer</u> coupled to the first processor and the second processor, <u>the first buffer being a register buffer;</u> <u>a second buffer</u> coupled to the first processor and the second processor, <u>the second buffer being a trace buffer</u>."

Hennessy discloses using scoreboarding to aid in allowing instructions to execute out of order. Sundaramoorthy, however, is directed to finding instructions that do not effect final program output and removes these instructions from a second stream, for example redundant instructions. Therefore, the combination of the two prior art documents would not result in Applicant's claimed invention. Further, Hennessy does not teach, disclose or suggest "the first processor executes a single threaded application ahead of the second processor executing said single threaded application to avoid misprediction."

Moreover, by viewing the disclosures of Sundaramoorthy and Hennessy, one can not jump to the conclusion of obviousness without <u>impermissible hindsight</u>. According

to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Applicant submits that without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to "the first processor executes a single threaded application ahead of the second processor executing said single threaded application to avoid misprediction," among other claimed limitations.

Neither Sundaramoorthy, Hennessy, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claims 1, 11, 20 and 29, as listed above. Since neither Sundaramoorthy, Hennessy, nor the combination of the two teach, disclose or suggest all the limitations of Applicant's amended claims 1, 11, 20 and 29, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 11, 20 and 29 are not obvious over Sundaramoorthy in view of Hennessy since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 11, 20 and 29, namely claims 2-7 and 9-10, 12-13, 21-27, and 30-35, respectively, would also not be obvious over Sundaramoorthy in view of Hennessy for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 1-7, 9-13, 17-19, 27 and 29-35 are respectfully requested.

B.   It is asserted in the Office Action that claims 14-16 and 23-25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Hennessy and in further view of Akkary (WO 99/31594). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's claims 14-16 indirectly depend on amended claim 11. As asserted above in section II, neither Sundaramoorthy, Hennessy, nor the combination of the two teach, disclose or suggest the limitations contained in Applicant's amended claims 11 and 20.

Akkary discloses a system for ordering loads and stores in a multithreaded processor using load and store buffers. Applicant is well aware of Akkary as Akkary is owned by Applicant's assignee. Akkary does not teach, disclose or suggest "executing a plurality of instructions in a first thread by a first processor; executing said plurality of instructions in the first thread by a second processor as directed by the first processor, the second processor executing said plurality of instructions ahead of the first processor to avoid misprediction," nor "executing a first thread from a first processor; executing said first thread from a second processor as directed by the first processor, the second processor executing instructions ahead of the first processor to avoid misprediction."

Neither Sundaramoorthy, Hennessy, Akkary, nor the combination of the three, teach, disclose or suggest the limitations contained in Applicant's amended claims 11 and 20, as listed above. Since neither Sundaramoorthy, Hennessy, Akkary, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's amended claims 11 and 20, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 11 and 20 are not obvious over Sundaramoorthy in view of Hennessy, and further in view of Akkary since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 11 and 20, namely claims 14-16, and 23-25, respectively, would also not be obvious over Sundaramoorthy in view of Hennessy and further in view of Akkary for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 14-16 and 23-25 are respectfully requested.

C.   It is asserted in the Office Action that claims 20-22, 26 and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sundaramoorthy in view of Hennessy and in further view of "Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12 ("Tanenbaum"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

Applicant has addressed amended claim 20 regarding Sundaramoorthy in view of Hennessy above in section II(A).

Tanenbaum is only relied on for asserting that "any instruction executed by hardware can also be executed in software." Tanenbaum, however, does not teach, disclose or suggest "executing a first thread from a first processor; executing said first thread from a second processor as directed by the first processor, the second processor executing instructions ahead of the first processor to avoid misprediction."

Neither Sundaramoorthy, Hennessy, Tanenbaum, nor the combination of the three, teach, disclose or suggest the limitations contained in Applicant's amended claim 20, as listed above. Since neither Sundaramoorthy, Hennessy, Tanenbaum, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's amended claim 20, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 20 is not obvious over Sundaramoorthy in view of Hennessy and further in view of Tanenbaum since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 20, namely claims 21-22, 26 and 28, would also not be obvious over Sundaramoorthy in view of Hennessy and further in view of Tanenbaum for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 20-22, 26 and 28 is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-7 and 9-35, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: <u>November 19, 2004</u>

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Jean Svoboda